WHAT IS CLAIMED IS:

1. A gate driver integrated circuit for switching a power transistor using an external supply voltage and an external controller, comprising:

an output stage configured to be coupled to the power transistor and to detect a desaturation state of the power transistor and to execute a soft shutdown sequence to gradually shut down the power transistor, such that transient over-voltage of the power transistor is prevented during the soft shutdown sequence;

an input stage coupled to the output stage and configured to be coupled to the external controller via an external control input, the input stage being configured to control the output stage as a function of the external control input during normal operation; and

a fault control circuit coupled to the output stage and the input stage, the fault control circuit being operable to place the input stage in a hold state during the soft shutdown sequence, such that the input stage ignores the external control input during the soft shutdown sequence, wherein the fault control circuit, the input stage and the output stage are integrated in the integrated circuit.

2. The integrated circuit of claim 1, further comprising an under-voltage protection circuit coupled to the fault control circuit and the under-voltage protection circuit being operable to detect an under-voltage state of the external supply voltage.

3. The integrated circuit of claim 2, wherein the fault control circuit is operably configured to initiate a shutdown of the output stage in response to the detection of the under-voltage state of the external supply voltage by the under-voltage protection circuit.

4. The integrated circuit of claim 3, wherein, during the soft shutdown sequence, the fault control circuit is operably configured to delay initiating the shutdown of the output stage in response to the detection of the under-voltage state of the external supply by the under-voltage protection circuit.

5. The integrated circuit of claim 1, wherein the output stage is coupled to the power transistor by an external sourcing connection, an external sinking connection and an external soft shutdown connection.

6. The integrated circuit of claim 4, wherein the fault control circuit is configured to be coupled to a dedicated local network, and the fault control circuit is operably configured to detect an external desaturation fault signal communicated on the dedicated local network.

7. The integrated circuit of claim 6, wherein the fault control circuit is operably configured to place the input stage in the hold state when the fault control circuit detects the external desaturation fault on the dedicated local network.

8. The integrated circuit of claim 7, wherein the fault control circuit is operably configured to communicate a desaturation fault signal on the dedicated local network during the soft shutdown sequence.

9. The integrated circuit of claim 8, wherein the dedicated local network is not connected to the external controller.

10. The integrated circuit of claim 9, wherein the fault control circuit is configured to be coupled to the dedicated local network using a common external

desaturation fault signal input-output connection, such that the external desaturation fault signal communicated on the dedicated local network uses the common external desaturation fault signal input-output connection.

11. The integrated circuit of claim 10, wherein the fault control circuit is configured to be coupled to a shutdown fault network, the fault control circuit being operable to detect an external shutdown fault on the shutdown fault network and to communicate an external shutdown fault on the shutdown fault network.

12. The integrated circuit of claim 11, wherein, during the normal operation, the fault control circuit is operably configured to communicate an external shutdown fault signal on the shutdown fault network in response to the detection of the under-voltage state of the external supply voltage by the under-voltage protection circuit.

13. The integrated circuit of claim 12, wherein, during the soft shutdown sequence, the fault control circuit is configured to delay the communicating of the external shutdown fault signal in response to the detection of the under-voltage state of the external supply voltage by the under-voltage protection circuit, until the soft shutdown sequence is completed by the output stage.

14. The integrated circuit of claim 13, wherein the fault control circuit is configured to latch the external shutdown fault signal on the shutdown fault network after completion of any soft shutdown sequence.

15. The integrated circuit of claim 14, wherein the fault control circuit is configured to be operably coupled to the external controller, the fault control circuit

operably detecting an external fault clear signal communicated by the external controller.

16. The integrated circuit of claim 17, wherein the fault control circuit is configured to unlatch the external shutdown fault signal, after the external shutdown fault signal is latched by the fault control circuit after the soft shutdown sequence is completed, only when the external fault clear signal is communicated by the external controller.

17. The integrated circuit of claim 16, wherein the external fault clear signal is an active high signal.

18. The integrated circuit of claim 17, wherein the external shutdown fault signal is an active low signal.

19. The integrated circuit of claim 17, wherein the external desaturation fault signal is active low, when asserted on the dedicated local network.

20. A gate driver integrated circuit for switching a first power transistor and a second power transistor using an external controller and an external supply voltage, the external supply voltage being capable of being bootstrapped from a floating supply voltage, the integrated circuit comprising:

a first output stage configured to be coupled to the first power transistor and to detect a desaturation state of the first power transistor and to execute a soft shutdown sequence of the first output stage to gradually shut down the first power transistor, such that a transient over-voltage of the first power transistor is prevented during the soft shutdown sequence;

a second output stage configured to be coupled to the second power transistor and to detect a desaturation state of the second output stage and to execute a soft shutdown sequence of the second power transistor to gradually shut down the second power transistor, such that transient over-voltage of the second power transistor is prevented during the soft shutdown sequence;

an input stage coupled to the first output stage and the second output stage and configured to be coupled to the external controller via a first external control input and a second external control input, and during normal operation, the input stage is configured to control the first output stage as a function of the first external control input and the second output stage as a function of the second external control input; and

a fault control circuit coupled to the first output stage, the second output stage and the input stage, the fault control circuit being operable to place the input stage in a hold state during the soft shutdown sequence of the first output stage, the second output stage or both the first and second output stages, such that the input stage ignores the first external control input and the second external control input during the soft shutdown sequence of the first output stage, the second output stage or both the first and second output stages, wherein the fault control circuit, the input stage, the second output stage and the first output stage are integrated in the integrated circuit.

21. The integrated circuit of claim 20, further comprising:

a first under-voltage protection circuit coupled to the fault control circuit and the under-voltage protection circuit being operable to detect an under-voltage state of the external supply voltage, such that the fault control circuit is operably configured to initiate a shutdown of both the first output stage and the second output stage in

response to the detection of the under-voltage state of the external supply voltage by the under-voltage protection circuit.

22. The integrated circuit of claim 21, further comprising:

a second under-voltage protection circuit coupled to the second output stage and configured to detect an under-voltage state of the floating supply voltage, such that the second output stage initiates a shutdown of the second output stage, when an under-voltage state of the floating supply voltage is detected.

23. The integrated circuit of claim 22, wherein the second under-voltage protection circuit and the second output stage are configured such that the first output stage continues to control the second power transistor and to generate diagnostic signals.

24. The integrated circuit of claim 23, wherein the fault control circuit manages fault states using three external fault connections, including a desaturation fault input-output connection configured to couple to a dedicated local network, a shutdown fault input-output connection configured to couple to a shutdown fault network including the external controller, and a fault clear input connection configured to couple to the external controller.

25. The integrated circuit of claim 24, wherein the fault control circuit is configured to detect the desaturation fault signal on the dedicated local network and the shutdown fault signal on the shutdown fault network.

26. The integrated circuit of claim 25, wherein the fault control circuit includes fault management logic such that the fault control circuit asserts a

desaturation fault on the dedicated local network during the soft shutdown sequence of the first output stage, the second output stage or both the first and second output stages and latches active a shutdown fault on the shutdown fault network after the soft shutdown sequence of the first output stage, the second output stage or both the first and second output stages is completed, wherein assertion of the fault clear input by the external controller is required to unlatch the shutdown fault of the fault control logic.

27. The integrated circuit of claim 26, wherein the fault control circuit is configured such that the shutdown fault is asserted on the shutdown fault network, but not latched, during detection of an under-voltage state of the supply voltage by the first under-voltage protection circuit, and when a shutdown fault is asserted on the shutdown fault network, the fault control circuit detects the shutdown fault initiates a shutdown of the first output stage and the second output stage, unless the desaturation fault is asserted on the dedicated local network, wherein the desaturation fault takes priority over the shutdown fault.

28. The gate driver integrated circuit of claim 24, wherein the integrated circuit is configured such that an external bootstrap capacitor may be coupled to the second output stage and an external diode may be coupled between the output stage and the second under-voltage protection circuit, such that the external supply voltage is bootstrapped from the floating supply voltage, wherein the external supply voltage is fixed at a voltage greater than a minimum threshold voltage during the normal operation.

29. The gate driver integrated circuit of claim 28, wherein the floating supply voltage is capable of floating to 1200 Volts, and the first output stage is referenced to ground.

30. The gate driver integrated circuit of claim 29, wherein each of the power transistors are isolating gate bipolar transistors, and desaturation detection for each of the first output stage and the second output stage is suspended during a blanking time during transistor turn-on, wherein the blanking time is selected to be greater than the switching time, defined as the time spent to reach a plateau voltage for the isolating gate bipolar transistors.

31. The gate driver integrated circuit of claim 30, wherein the blanking time is no greater than 3 microseconds.

32. The gate driver integrated circuit of claim 30, wherein each of the output stages include a desaturation noise filter, such that the duration of the desaturation state must exceed a minimum pulse width before desaturation is detected.

33. The gate driver integrated circuit of claim 31, wherein the minimum pulse width is at least 1 microsecond.

34. A gate driver integrated circuit for switching a low side transistor and a high side transistor using an external logic supply voltage, an external floating supply voltage and an external controller, comprising:

an input stage configured to couple to the external controller, the external controller communicating a low side input signal and a high side input signal to the input stage, the input stage comprising an internal hold stage receiving a hold signal

and an internal switching stage receiving a shutdown signal, the hold stage placing the input stage in a hold state when a hold signal is received, such that the low side input signal and the high side input signal are held by the hold stage, preventing further communication of the signals to the switching stage, the switching stage communicating a shutdown to both of the high side output stage and the low side output stage when the shutdown signal is received by the shutdown stage;

a level shifter coupled to the switching stage;

a high side output stage configured to be externally coupled to the high side transistor, the high side output stage being internally coupled to the level shifter to receive a high side switching signal, such that the high side transistor is switched on when the high side switching signal is received, the high side output stage comprising protection circuitry and a predriver, the predriver controlling switching of the high side transistor during normal operation, and the protection circuitry of the high side output stage operably detecting an under-voltage state of the high side supply voltage and a desaturation of the high side transistor, and the protection circuitry of the high side output stage shutting off the high side transistor when the under-voltage state of the high side supply voltage is detected and protecting the high side transistor when the desaturation of the high side transistor is detected, such that the high side transistor is gradually turned off, avoiding transient over-voltage states;

a low side output stage coupled to the switching stage to receive a low side switching signal and configured to be coupled to the low side transistor, such that the low side transistor is switched on when the low side switching signal is received by the low side output stage, the low side output stage comprising protection circuitry and a predriver, the predriver controlling switching of the low side transistor during normal operation, and the protection circuitry of the low side output stage detecting desaturation of the high side transistor, and the protection circuitry of the low side output stage protecting the high side transistor when desaturation of the high side

transistor is detected such that the high side transistor is gradually turned off, avoiding transient over-voltage states;

a logic supply under-voltage protection circuit configured to detect an under-voltage state of the logic supply voltage and to communicate a logic supply under-voltage signal; and

a fault control circuit, the fault control circuit is coupled to the hold stage, the switching stage, the low side output stage, the high side output stage, and the logic supply under-voltage protection circuit, and the fault control circuit is configured to be coupled to the external controller and an external dedicated local network, and the the fault control circuit is configured to manage signals received from the external controller, the external dedicated local network, the logic supply under-voltage protection circuit, the high side output stage and the low side output stage such that the fault control circuit communicates the internal hold signal to the input stage when a desaturation signal is communicated by one of the external dedicated local network, the high side output stage and the low side output stage, and only when the desaturation signal is communicated by one of the high side output stage and the low side output stage, the fault control circuit latches both the internal shutdown signal and an external shutdown signal when the desaturation protection is completed and communication of the desaturation signal is terminated, and when the external controller has communicated a fault clear signal to the fault control circuit, resetting the fault controller and no subsequent communication of the desaturation signal has been received from one of the external dedicated local network, the high side output stage and the low side output stage, the fault control network is configured to communicate the internal shutdown signal to the switching stage when the logic supply under-voltage signal is communicated by logic supply under-voltage protection circuit, initiating shutdown of both of the high side transistor and the low side transistor.

35. A multi-phase system of gate drivers for a multi-phase power supply using one gate driver integrated circuit of claim 28 for each phase of the multi-phase power supply.